CLAIMS

What is claimed is:

1. A process for forming a nonvolatile memory comprising:

providing a substrate;

identifying a first area of the substrate for a memory array and a second area of the substrate for a reference transistor;

forming a first dielectric layer overlying the substrate;

forming a storage material layer overlying the first dielectric layer;

forming a second dielectric layer overlying and surrounding the storage material layer;

forming a first barrier layer overlying the second dielectric layer;

providing a pattern to selectively remove the first barrier layer, the first and second dielectric layers and the storage material layer from all areas except above the first area of the substrate;

forming a third dielectric layer overlying the second area of the substrate and overlying the first barrier layer above the first area of the substrate;

forming a fourth dielectric layer overlying the third dielectric layer above the first area of the substrate and the second area of the substrate;

forming a second barrier layer overlying the fourth dielectric layer;

selectively removing the second barrier layer, the third dielectric and the fourth dielectric everywhere except overlying the second area of the substrate;

removing the first barrier layer overlying the first area of the substrate and removing the second barrier layer overlying the second area of the substrate;

forming a conductive gate layer overlying the second dielectric in the first area of the substrate and overlying the fourth dielectric in the second area of the substrate;

patterning gate stacks of transistors in the first area of the substrate and a reference gate stack in the second area of the substrate; and

forming current electrode regions in the first area of the substrate and the second area of the substrate to form memory cells in the first area of the substrate and a reference transistor in the second area of the substrate.

2. The process of claim 1 wherein forming the storage material layer further comprises forming a layer of nanoclusters.

3. The process of claim 2 wherein the forming of nanoclusters further comprises forming dots comprising at least one of silicon, nitride, germanium, silver, platinum, gold, tungsten, and tantalum that are spaced apart at least in some regions so as to not be in direct contact.

4. The process of claim 1 further comprising:

identifying a third area of the substrate to form other circuitry for communication with the nonvolatile memory.

5. The process of claim 1 further comprising:

implementing the first area of the substrate in a first well region having a first doping concentration;

implementing the second area of the substrate in a second well region having a second doping concentration; and

implementing the first doping concentration to be substantially equal to the second doping concentration.

6. The process of claim 1 further comprising:

implementing the first area of the substrate in a first well region having a first doping concentration;

implementing the second area of the substrate in a second well region having a second doping concentration; and

implementing the first doping concentration to be different from the second doping concentration.

7. A process for forming a nonvolatile memory comprising:

providing a substrate having a first region for a memory array and a second region for a reference transistor;

forming a plurality of memory cell transistors in the first region of the substrate, each of the plurality of memory cell transistors comprising a gate stack structure comprising a gate dielectric and a layer of storage material having a predetermined height; and

forming the reference transistor in the second region of the substrate, the reference transistor having a reference transistor gate stack structure comprising a first dielectric

layer and a second dielectric layer, the first dielectric and the second dielectric collectively permitting the threshold voltage of the reference transistor to vary with respect to program and erase operations of the nonvolatile memory over time.

8. The process of claim 7 further comprising:

implementing the first dielectric layer and the second dielectric layer with a material of substantially a same composition but formed by differing formation methods.

9. The process of claim 7 further comprising:

implementing the first dielectric layer and the second dielectric layer with materials of differing composition.

10. The process of claim 7 further comprising:

implementing the layer of storage material within the plurality of memory cell transistors by providing nanocrystals that have at least some regions where the nanocrystals are physically spaced apart.

11. The process of claim 7 further comprising:

implementing the reference transistor so that the first dielectric layer and the second dielectric layer collectively have a height substantially equal to the predetermined height.

12. A nonvolatile memory comprising:

a substrate, wherein a first area of the substrate is for a memory array and a second area of the substrate is for a reference transistor;

gate stack structures overlying the first area of the substrate, each of the gate stack structures comprising a first dielectric layer overlying the substrate, a storage material layer overlying the first dielectric layer, a second dielectric layer overlying and surrounding the storage material layer, and a gate material overlying the second dielectric layer; and

the reference transistor having a reference transistor gate stack structure comprising a third dielectric layer and a fourth dielectric layer, the third dielectric and the fourth dielectric collectively permitting a threshold voltage of the reference transistor to vary with respect to program and erase operations of the nonvolatile memory over time, the reference transistor further comprising the gate material overlying the fourth dielectric layer.

13. The nonvolatile memory of claim 12 wherein the first dielectric, the second dielectric, the third dielectric and the fourth dielectric are comprised of differing compositions.

14. The nonvolatile memory of claim 12 wherein the storage material layer further comprises nanoclusters of at least one of silicon, nitride, germanium, silver, platinum, gold, tungsten, and tantalum.

15. The nonvolatile memory of claim 12 further comprising:

a third area of the substrate, the third area containing other circuitry for use with the nonvolatile memory.

16. The nonvolatile memory of claim 12 further comprising:

diffusion regions formed in the first area of the substrate for forming source and drain regions for the gate stack structures.

17. The nonvolatile memory of claim 12 wherein the third dielectric layer and the fourth dielectric layer of the reference transistor permit the reference transistor to have a variable threshold voltage as a function of a number of times the reference transistor is biased.